

# COMPUTER ARCHITECTURE

<b>1</b>	Course Title:	COMPUTER ARCHITECTURE	
<b>2</b>	Course Code:	BMB3002	
<b>3</b>	Type of Course:	Compulsory	
<b>4</b>	Level of Course:	First Cycle	
<b>5</b>	Year of Study:	3	
<b>6</b>	Semester:	6	
<b>7</b>	ECTS Credits Allocated:	5.00	
<b>8</b>	Theoretical (hour/week):	3.00	
<b>9</b>	Practice (hour/week):	0.00	
<b>10</b>	Laboratory (hour/week):	0	
<b>11</b>	Prerequisites:	None	
<b>12</b>	Language:	Turkish	
<b>13</b>	Mode of Delivery:	Face to face	
<b>14</b>	Course Coordinator:	Dr. Öğr. Üyesi Metin BİLGİN	
<b>15</b>	Course Lecturers:		
<b>16</b>	Contact information of the Course Coordinator:	Bilgisayar Müh. Bölüm Binası, 1. kat, oda 3 Tel.:+90 (224) 275 52 63 email: metinbilgin at uludag.edu.tr	
<b>17</b>	Website:		
<b>18</b>	Objective of the Course:	Teaching basic ideas about modern computer architecture is the main aim. To teach concepts about CPU design and memory hierarchies.	
<b>19</b>	Contribution of the Course to Professional Development:		
<b>20</b>	Learning Outcomes:		
		1	Learns memory Hierarchy Design
		2	Learns Instruction-Level Parallelism
		3	Learns Data-Level Parallelism
		4	Learns Thread-Level Parallelism
		5	Learns Pipelining
		6	
		7	
		8	
		9	
		10	
<b>21</b>	Course Content:		
		<b>Course Content:</b>	
Week	Theoretical	Practice	
<b>1</b>	One processor and multiple processor systems-Ahmdal's law		
<b>2</b>	Memory management: Virtual memory systems, paging and segmentation		
<b>3</b>	Cache memory systems and replacement algorithms		
<b>4</b>	Pipeline processor design		

<b>5</b>	Feedback pipelines, reservation tables and collision vector	
<b>6</b>	A comparison of RISC-CISC architectures	
<b>7</b>	Shared memory multiprocessor systems and Flynn's classification	
<b>8</b>	Bus based multiprocessor systems: Crossbar switch and multi-gate memory	
<b>9</b>	Interconnected networks: a-Dynamic Interconnected networks: Multistage Networks (Omega Network) b-Static Interconnected networks: Star, Ring, Mesh, Hypercube and Tree network	
<b>10</b>	Message Passing Interface (MPI)	
<b>11</b>	Point-to-point Communication	
<b>12</b>	Collective Communication	
<b>13</b>	Parallel algorithms for vector-matrix multiplication and matrix transpose	
<b>14</b>	Fox and Cannon algorithms for matrix multiplication	
<b>22</b>	Textbooks, References and/or Other Materials:	Computer Architecture, A Quantitative Approach, John L. Hennessy and David A. Patterson, Fifth Edition
<b>23</b>	Assesment	
<b>TERM LEARNING ACTIVITIES</b>		
	<b>NUMBER</b>	<b>WEIGHT</b>
Midterm Exam	1	40.00
Quiz	0	0.00
Home work-project	0	0.00
Final Exam	1	60.00
Total	2	100.00
Contribution of Term (Year) Learning Activities to Success Grade		40.00
Contribution of Final Exam to Success Grade		60.00
Total		100.00
Measurement and Evaluation Techniques Used in the Course		
<b>24</b>	<b>ECTS / WORK LOAD TABLE</b>	

Activites	Number	Duration (hour)	Total Work Load (hour)
Theoretical	14	3.00	42.00
Practicals/Labs	0	0.00	0.00
Self study and preperation	14	7.00	98.00
Homeworks	0	0.00	0.00
Projects	0	0.00	0.00
Field Studies	0	0.00	0.00
Midterm exams	1	2.00	2.00
Others	0	0.00	0.00
Final Exams	1	2.00	2.00
Total Work Load			144.00
Total work load/ 30 hr			4.80
ECTS Credit of the Course			5.00

25	CONTRIBUTION OF LEARNING OUTCOMES TO PROGRAMME QUALIFICATIONS															
	PQ1	PQ2	PQ3	PQ4	PQ5	PQ6	PQ7	PQ8	PQ9	PQ10	PQ11	PQ12	PQ13	PQ14	PQ15	PQ16
ÖK1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ÖK2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ÖK3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ÖK4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ÖK5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
<b>LO: Learning Objectives    PQ: Program Qualifications</b>																
<b>Contribution Level:</b>	<b>1 very low</b>		<b>2 low</b>			<b>3 Medium</b>			<b>4 High</b>			<b>5 Very High</b>				