ADVANCED COMOUTER ARCHITECTURE

1	Course Title:	ADVANCED COMOUTER ARCHITECTURE
2	Course Code:	BM5137
3	Type of Course:	Optional
4	Level of Course:	Second Cycle
5	Year of Study:	1
6	Semester:	1
7	ECTS Credits Allocated:	6.00
8	Theoretical (hour/week):	3.00
9	Practice (hour/week):	0.00
10	Laboratory (hour/week):	0
11	Prerequisites:	None
12	Language:	Turkish
13	Mode of Delivery:	Face to face
14	Course Coordinator:	Prof. Dr. KEMAL FİDANBOYLU
15	Course Lecturers:	-
16	Contact information of the Course Coordinator:	e-posta: kfidan@uludag.edu.tr Uludağ Üniversitesi, Bilgisayar Mühendisliği Bölümü Görükle Kampüsü, 16059 Nilüfer, Bursa
17	Website:	
18	Objective of the Course:	Teaching the basic concepts about modern computer architecture is the main aim of the course.
19	Contribution of the Course to Professional Development:	Engineering Science: 85%; Engineering Design: 15%
20	Learning Outcomes:	
	1	Understand the fundamentals of quantitative digital design and analysis
	2	Examine memory hierarchy in digital design
	3	Examine memory hierachies in the ARM Cortex-A8 and Intel Core i7
	4	Examine ınstruction-level parallelism and its exploitation
	5	Examine the Intel Core i7 and ARM Cortex-A8
	6	Examine data-level parallelism in vector, SIMD, and GPU architectures
	7	Examine mobile versus server GPUs and Tesla versus Core i7
	8	Understand thread-level parallelism
	9	Examine multicore processors and their performance
	10	Examine the MIPS architecture and the MIPS R4000 pipeline
21	Course Content:	

Course Content:

Week	Theoretical	Practice
1	Fundamentals of Quantitative Design and Analysis	
2	Performance, Price, and Power	
3	Memory Hierarchy Design	

4	Memory Hierachies in the ARM Cortex-A8 and Intel Core i7	
5	Instruction-Level Parallelism and Its Exploitation	
6	The Intel Core i7 and ARM Cortex-A8	
7	Data-Level Parallelism in Vector, SIMD, and GPU Architectures	
8	Mobile versus Server GPUs and Tesla versus Core i7	
9	Thread-Level Parallelism	
10	Multicore Processors and Their Performance	
11	Warehouse-Scale Computers to Exploit Request-Level and Data-Level Parallelism	
12	A Google Warehouse-Scale Computer	
13	The MIPS Architecture	
14	The MIPS R4000 Pipeline	

22	Textbooks, References and/or Other Materials:	Textbook: J. L. Hennessy, D. A. Patterson, Computer Architecture: A Quantitative Approach, Morgan and Kauffman, 6th edition, 2017. Supplementary Textbook: Sarah Harris and David Harris, Digital Design and Computer Architecture, RISC-V Edition, Elsevier, 1st edition, 2021

Activites		Number	Duration (hour)	Total Work Load (hour)
TERM LEARNING ACTIVITIES	**NUMBER**	**WEIGHT**		
Theoretical		14	3.00	42.00
Practicals/Labs		0	0.00	0.00
Self-study and preperation	0	0.00	5.00	70.00
Homeworks		1	33.00	33.00
Projects		0	0.00	0.00
Field Studies		0	0.00	0.00
Contribution of Term (Year) Learning Activities to Success Grade		40.00	15.00	15.00
Others		0	0.00	0.00
Final Exams		1	20.00	20.00
Total Work Load				180.00
ECTS Credit of the Course				6.00

Quiz	0	0.00
Final Exam	1	60.00
Contribution of Final Exam to Success Grade		60.00
Total work load / 30hr		6.00

Measurement and Evaluation Techniques Used in the	Classical problem-solving ability will be measured in simulation, report writing and presentation on a subject related to the course content.

24	**ECTS / WORK LOAD TABLE**

25	**CONTRIBUTION OF LEARNING OUTCOMES TO PROGRAMME QUALIFICATIONS**															
	PQ1	**PQ2**	**PQ3**	**PQ4**	**PQ5**	**PQ6**	**PQ7**	**PQ8**	**PQ9**	**PQ10**	**PQ11**	**PQ12**	**PQ13**	**PQ14**	**PQ15**	**PQ16**
ÖK1	5	3	3	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK2	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK3	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0

ÖK4	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK5	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK6	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK7	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK8	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK9	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0
ÖK10	5	4	4	2	2	2	0	0	0	0	0	0	0	0	0	0

LO: Learning Objectives PQ: Program Qualifications

Contribution Level:	**1 very low**	**2 low**	**3 Medium**	**4 High**	**5 Very High**