DIGITAL DESIGN

1	Course Title:	DIGITAL DESIGN
2	Course Code:	EMEZ104
3	Type of Course:	Compulsory
4	Level of Course:	Short Cycle
5	Year of Study:	1
6	Semester:	2
7	ECTS Credits Allocated:	4.00
8	Theoretical (hour/week):	3.00
9	Practice (hour/week):	0.00
10	Laboratory (hour/week):	1
11	Prerequisites:	None
12	Language:	Turkish
13	Mode of Delivery:	Face to face
14	Course Coordinator:	Öğr.Gör. ERCAN YAVUZ
15	Course Lecturers:	İsmet GÜCÜYENER
16	Contact information of the Course Coordinator:	İsmet GÜCÜYENER ismetguc@uludag.edu.tr, 02242942349, U.Ü. TBMYO Mekatronik Prg. Bşk. Görükle Bursa
17	Website:	
18	Objective of the Course:	In this course, aimed to gain knowledge and skills for to make install and run of digital logic circuit design, sequential control circuits, counter circuits, register circuits, ADC and DAC circuits.
19	Contribution of the Course to Professional Development:	
20	Learning Outcomes:	

	1	Being able to use of digital logic circuit elements
	2	Being able to prepare logic table of stated problem
	3	Being able to write logical function in simplified form.
	4	Being able to use combinational logic circuits
	5	Being able to use register circuits
	6	Being able to use flip-flop circuits
	7	Being able to design stated counter circuits
	8	Being able to use ADC circuits
	9	
	10	

21 Course Content:

Course Content:

Week	Theoretical	Practice
1	Elements of digital logic circuit	Introduction of laboratory
2	Digital logic circuits	Measurement devices and technique of logic circuit
3	Design of digital logic circuit	To obtain of gate element using of other gate elements
4	Combinational logic circuits	Logic circuit to voting of three person
5	Encoders, Decoders	Logic circuit to combination lock
6	Multiplexers, demultiplexers	Design of encoder with NAND gates

7	Flip-Flops	Decimal counter circuit
8	Repeating courses first midterm	Decoder circuit with 74LS138
9	Synchronous counters	Decoder circuit with 74LS138
10	Synchronous counters	Demultiplexer circuit with 74LS138
11	Registers	0 to 9 counter circuit with 7490
12	Asynchronous counters	ADC circuit
13	Repeating courses second midterm	ADC circuit
14	ADC and DAC circuits	DAC circuit
22	Textbooks, References and/or Other Materials:	Course notes, Digital Design (M. Morris Mano)
23	Assesment	

TERM LEARNING ACTIVITIES	**NUMBER**	**WEIGHT**
Midterm Exam	2	50.00
Quiz	0	0.00
Home work-project	0	0.00
Final Exam	1	50.00
Total	3	100.00
Contribution of Term (Year) Learning Activities to Success Grade		50.00
Contribution of Final Exam to Success Grade		50.00
Total		100.00
Measurement and Evaluation Techniques Used in the Course		

24 ECTS / WORK LOAD TABLE

Activites	Number	Duration (hour)	Total Work Load (hour)
Theoretical	14	2.00	28.00
Practicals/Labs	14	2.00	28.00
Self study and preperation	14	2.00	28.00
Homeworks	0	0.00	0.00
Projects	0	0.00	0.00
Field Studies	0	0.00	0.00
Midterm exams	2	10.00	20.00
Others	0	0.00	0.00
Final Exams	1	20.00	20.00
Total Work Load			124.00
Total work load/ 30 hr			4.13
ECTS Credit of the Course			4.00

25 CONTRIBUTION OF LEARNING OUTCOMES TO PROGRAMME QUALIFICATIONS

	PQ1	**PQ2**	**PQ3**	**PQ4**	**PQ5**	**PQ6**	**PQ7**	**PQ8**	**PQ9**	**PQ10**	**PQ11**	**PQ12**	**PQ13**	**PQ14**	**PQ15**	**PQ16**
ÖK1	0	0	0	0	5	5	4	3	0	5	4	0	0	0	0	0

ÖK2	0	0	0	0	4	5	4	3	0	4	5	0	0	0	0	0
ÖK3	1	0	1	4	5	5	2	3	2	5	4	0	0	0	0	0
ÖK4	0	1	1	2	3	5	3	2	1	4	4	0	0	0	0	0
ÖK5	0	0	0	1	5	5	3	3	2	4	2	0	0	0	0	0
ÖK6	1	1	0	3	5	5	4	3	3	4	4	0	0	0	0	0
ÖK7	1	1	2	2	4	5	4	2	3	5	5	0	0	0	0	0
ÖK8	1	2	1	2	5	5	5	5	4	5	5	0	0	0	0	0

LO: Learning Objectives PQ: Program Qualifications

Contribution Level:	**1 very low**	**2 low**	**3 Medium**	**4 High**	**5 Very High**